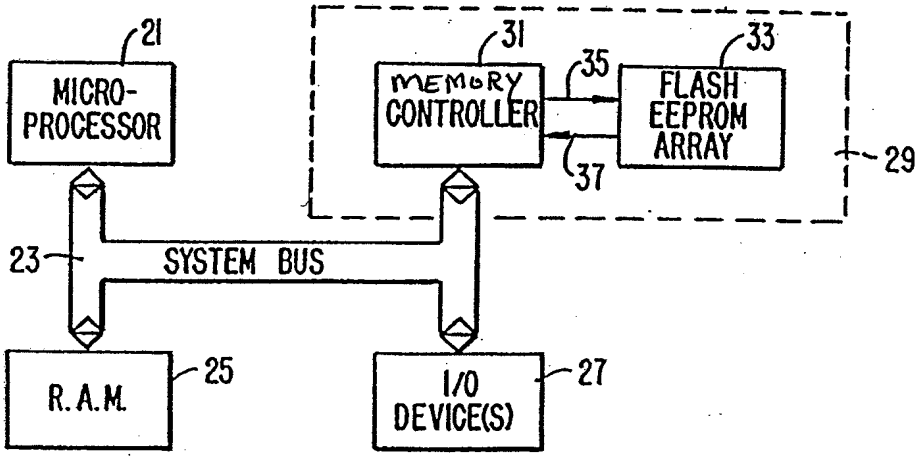

FIG._1A add "memory"

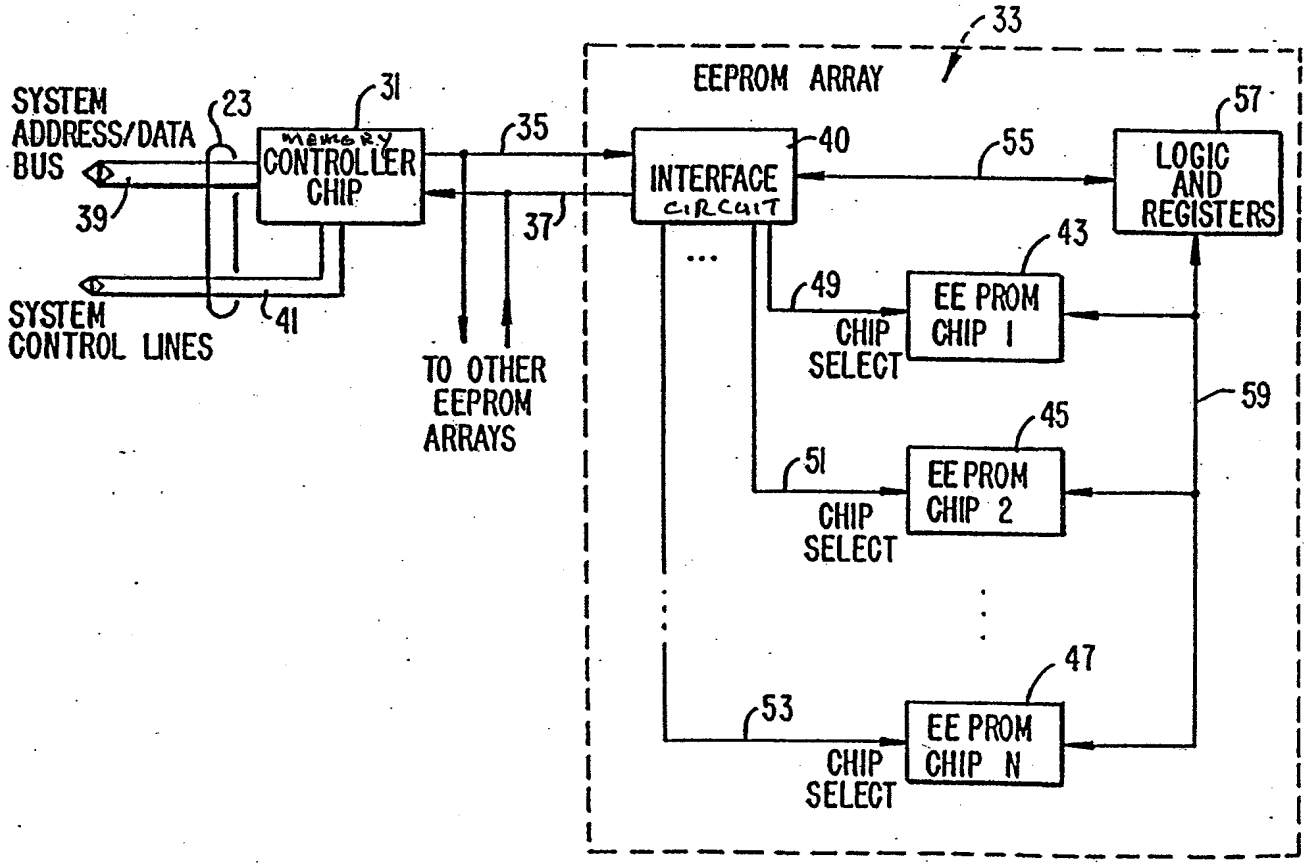

FIG._1B add "memory" + "circuit"

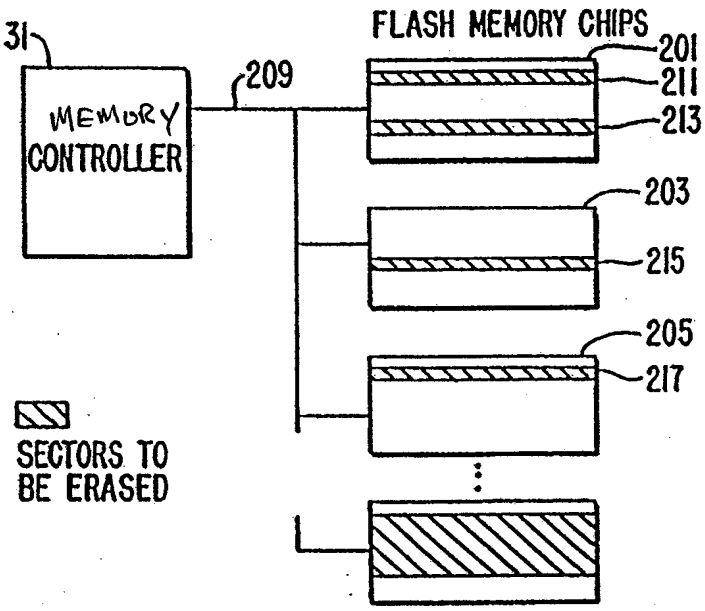

FIG._2 add "memory"

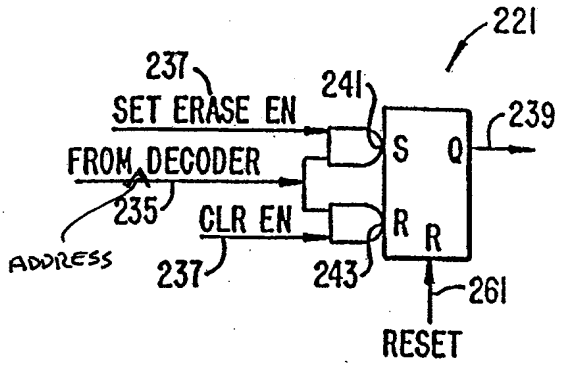

FIG._3B
add "ADDRESS"
(or "DECODER" → "ADDR DEC" is not enough room

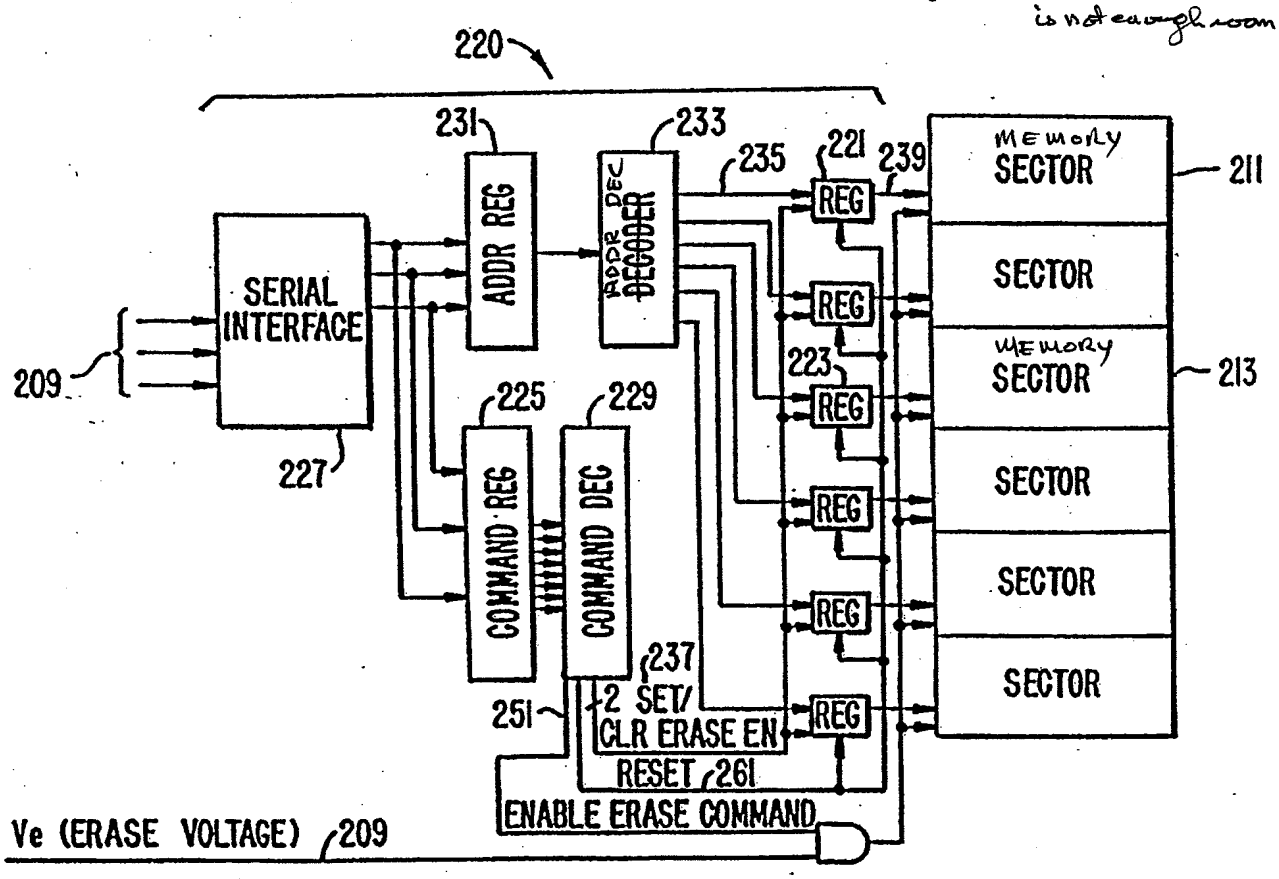

FIG._3A "DECODER" → "ADDR DEC"
add "MEMORY" x2

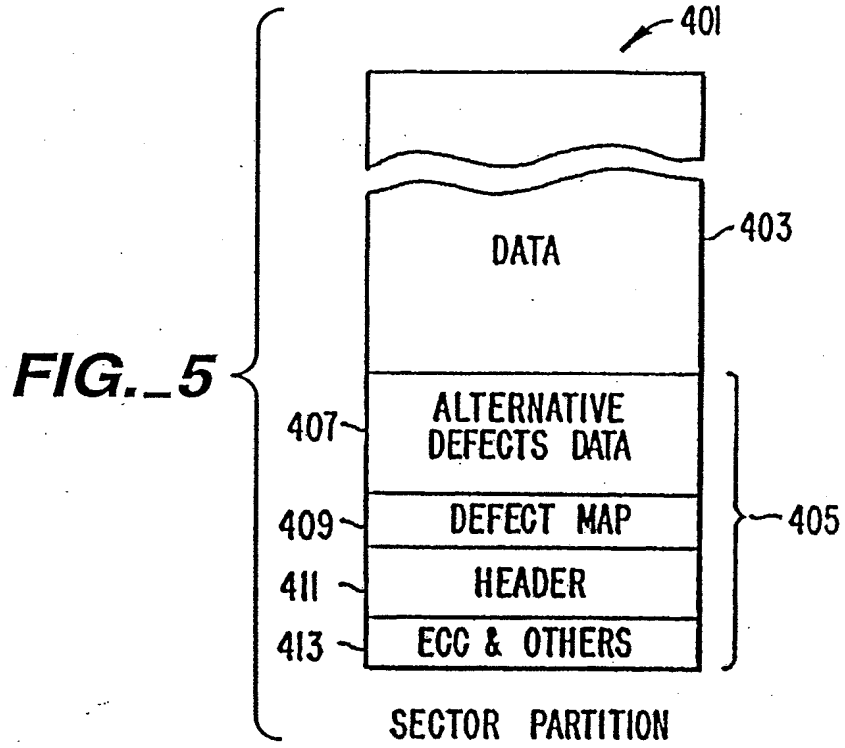

FIG._5

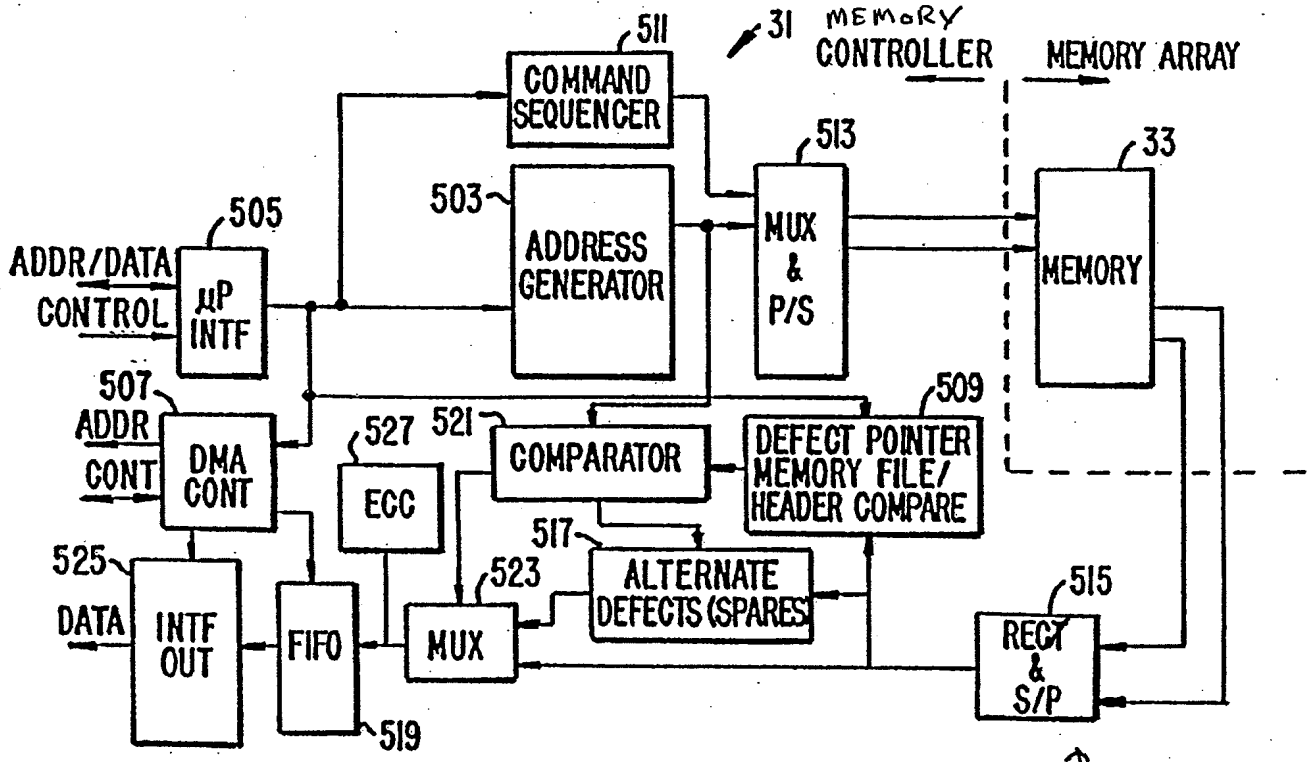

FIG._6

ADD "MEMORY", STRIKE "T" in "RECT"

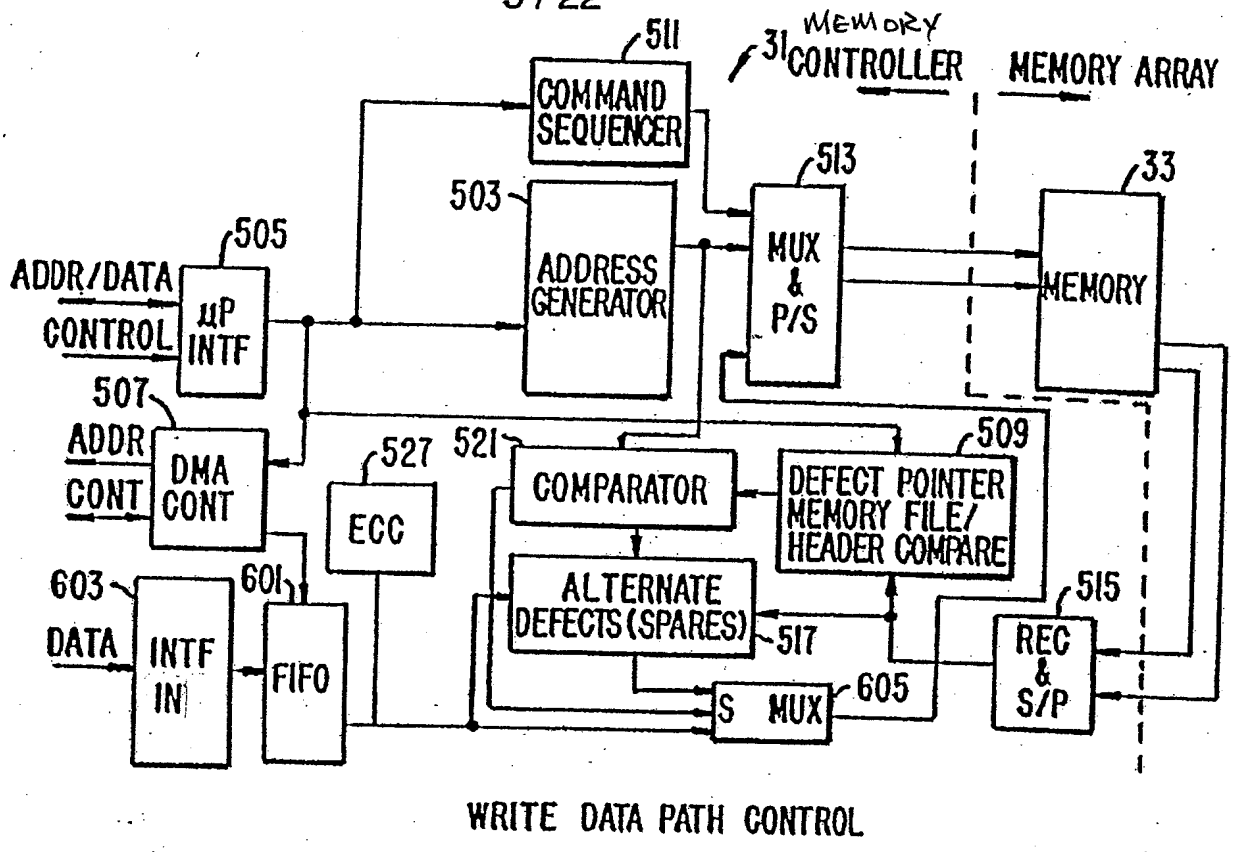

FIG._7 add " MEMORY

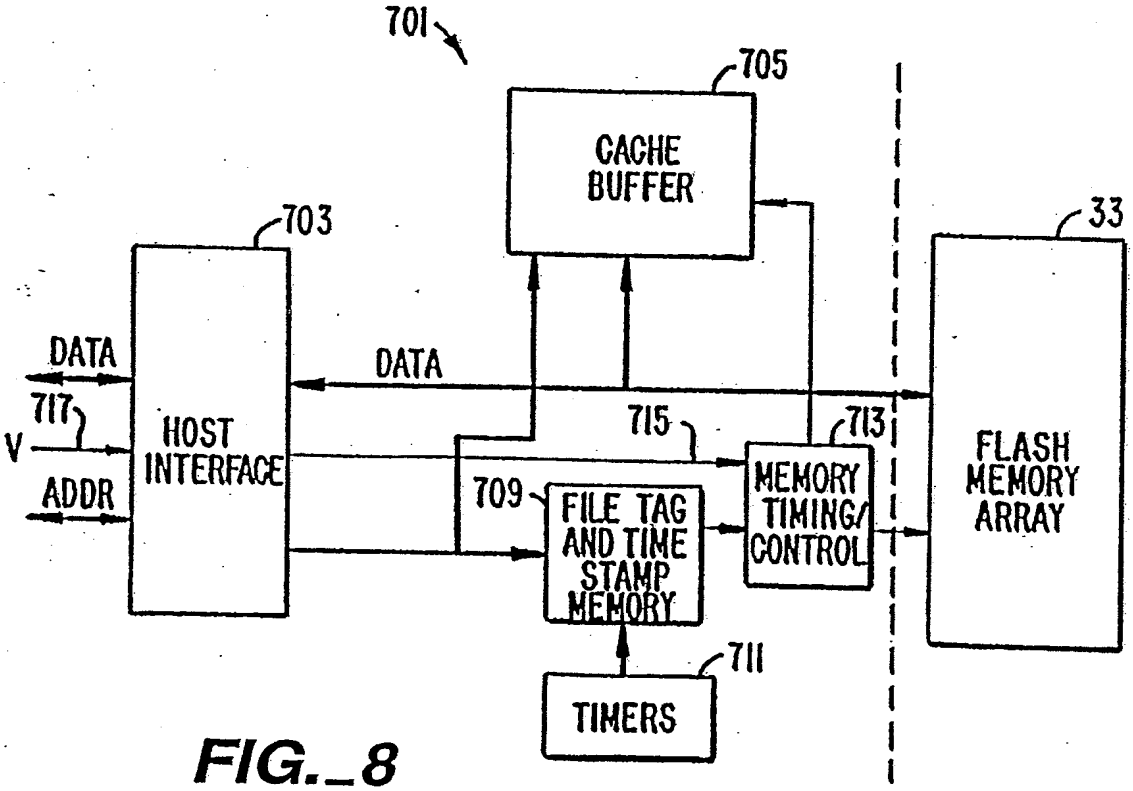

FIG._8

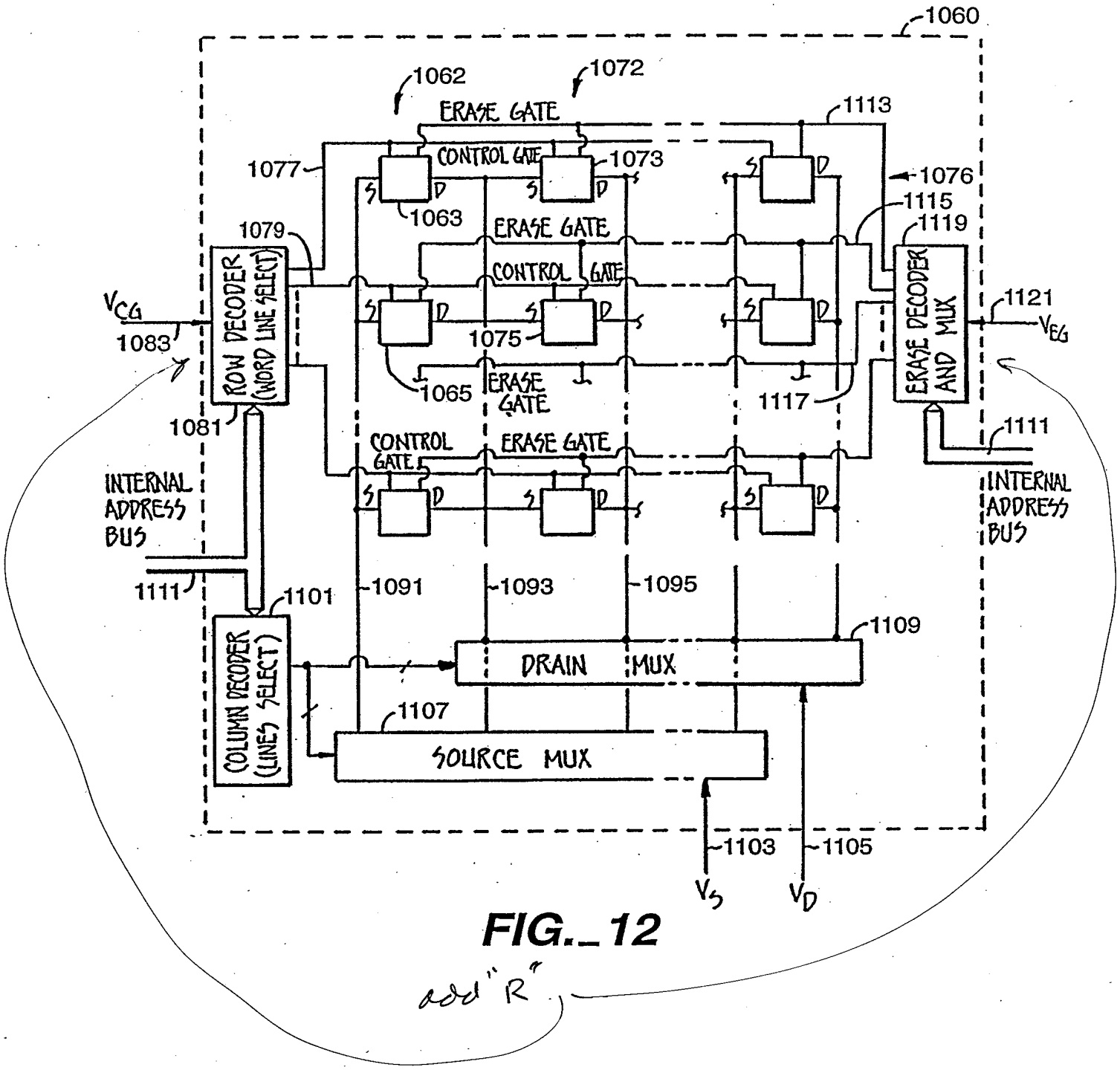
1060
1062
1072
ERASE GATE
1113
CONTROL GATE
1073
1077
1076
1063
1115
ERASE GATE
1119
1079
CONTROL GATE
ROW DECODER (WORD LINE SELECT)
ERASE DECODER AND MUX
V_{CG}
1121
V_{EG}
1083
1075
1065
ERASE GATE
1117
1081
1111
CONTROL GATE
ERASE GATE
INTERNAL ADDRESS BUS
INTERNAL ADDRESS BUS
1111
1101
1091
1093
1095
1109
DRAIN MUX
COLUMN DECODER (LINES SELECT)
1107
SOURCE MUX
1103
1105
V_S
V_D

FIG._12

add "R"

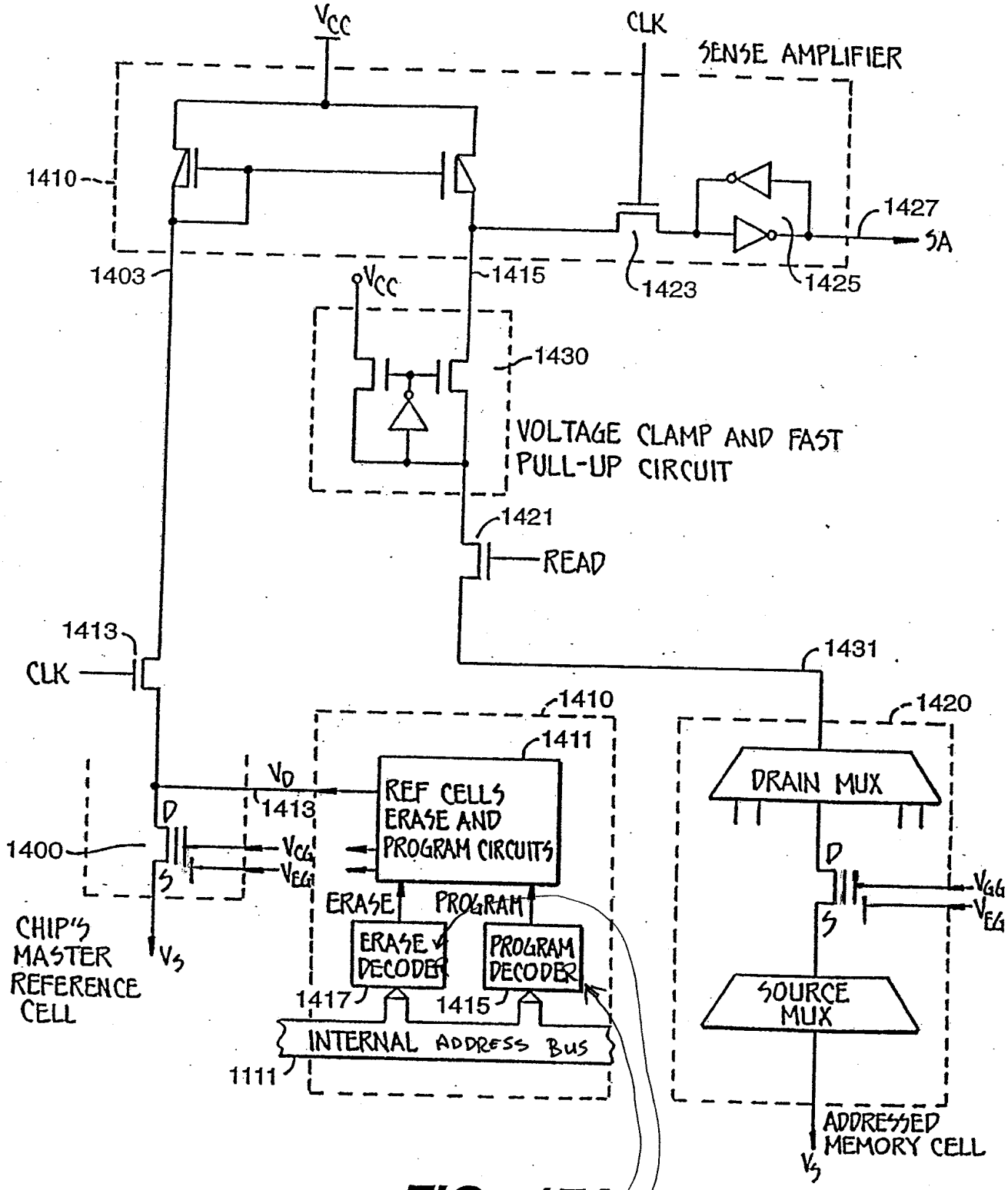

FIG._17A

add "R"

add "ADDRESS BUS"

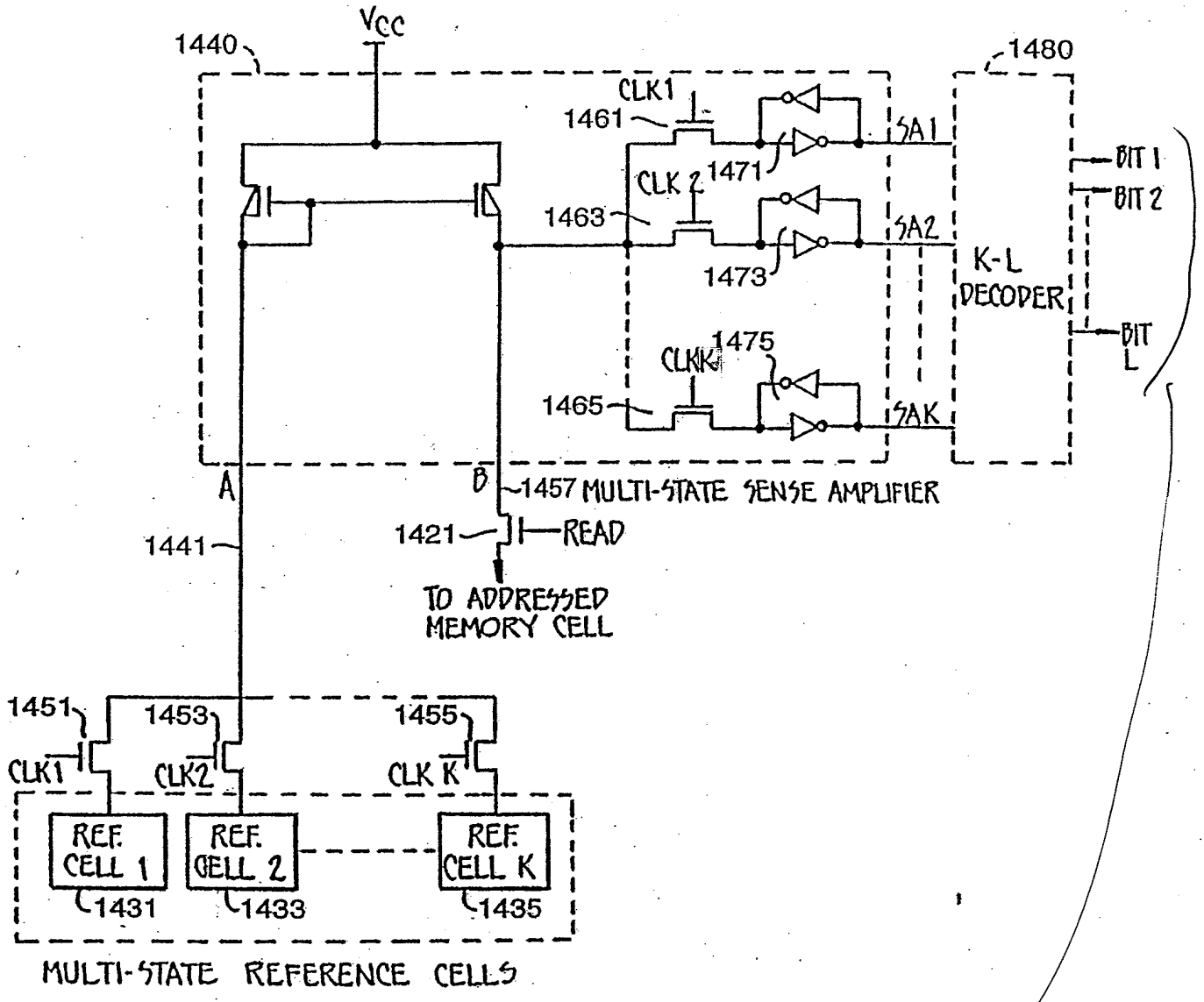

FIG._17B

Change "BIT" → "READ DATA BIT"